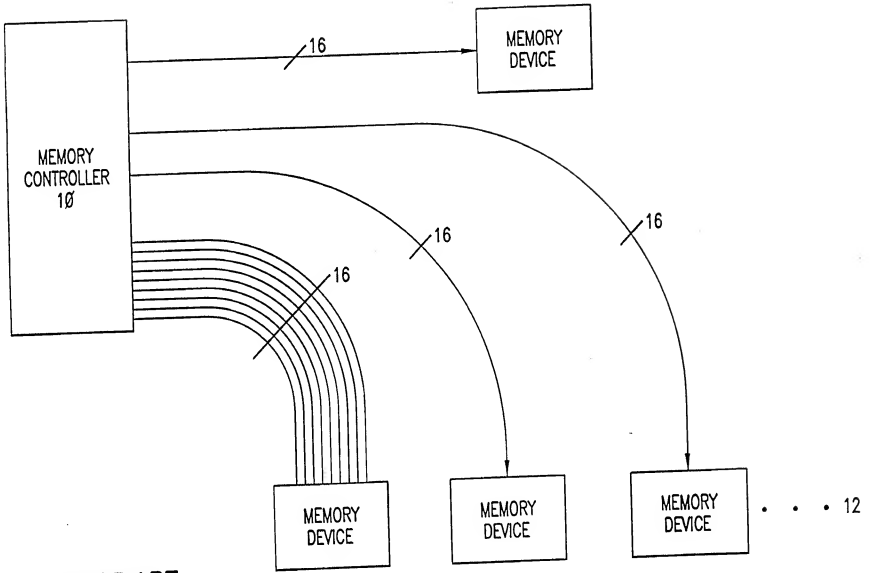
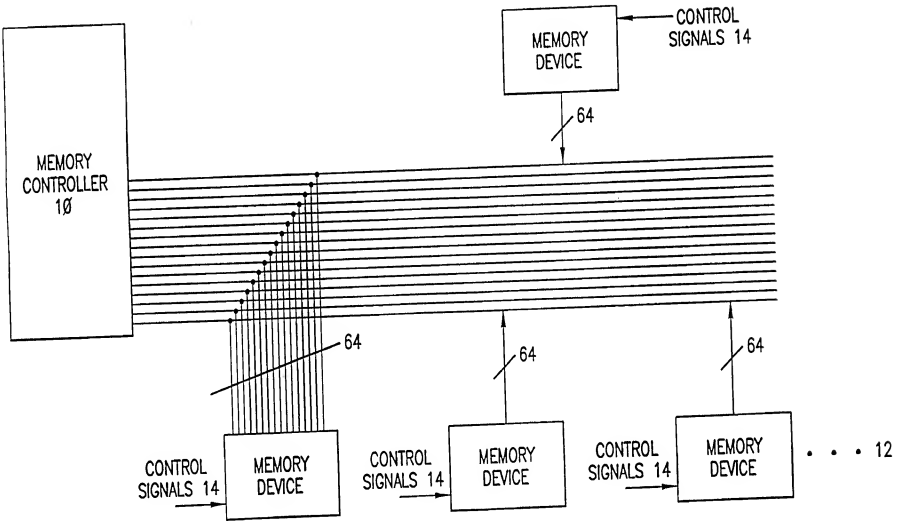


PRIOR ART

FIG. 1



PRIOR ART

FIG. 2

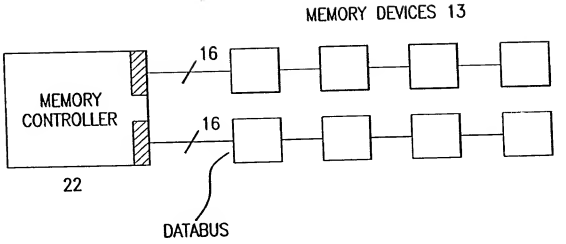


FIG.3

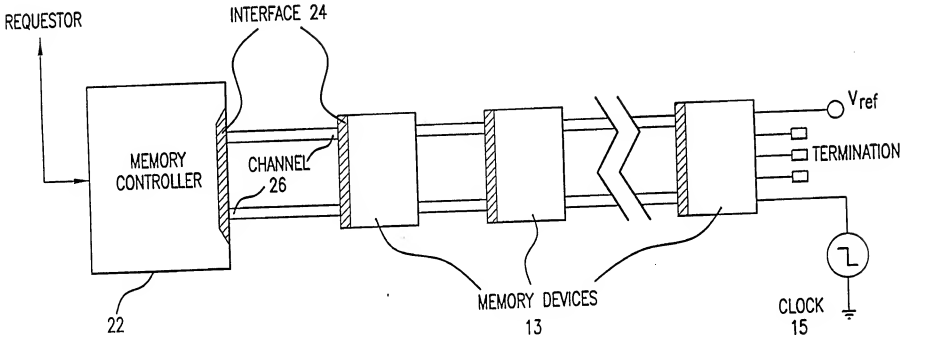

REQUESTOR
INTERFACE 24
MEMORY CONTROLLER
CHANNEL 26
22
MEMORY DEVICES 13
Vref
TERMINATION
CLOCK 15

FIG.4

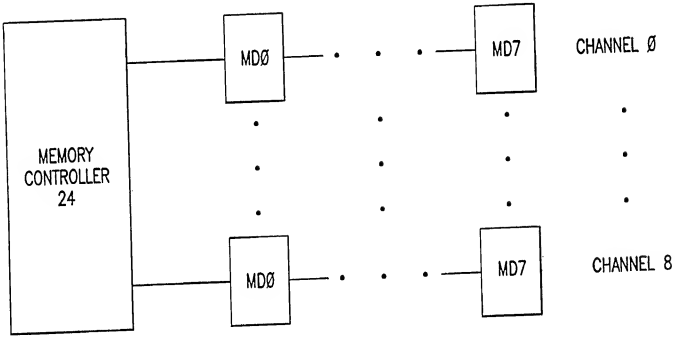


FIG. 5

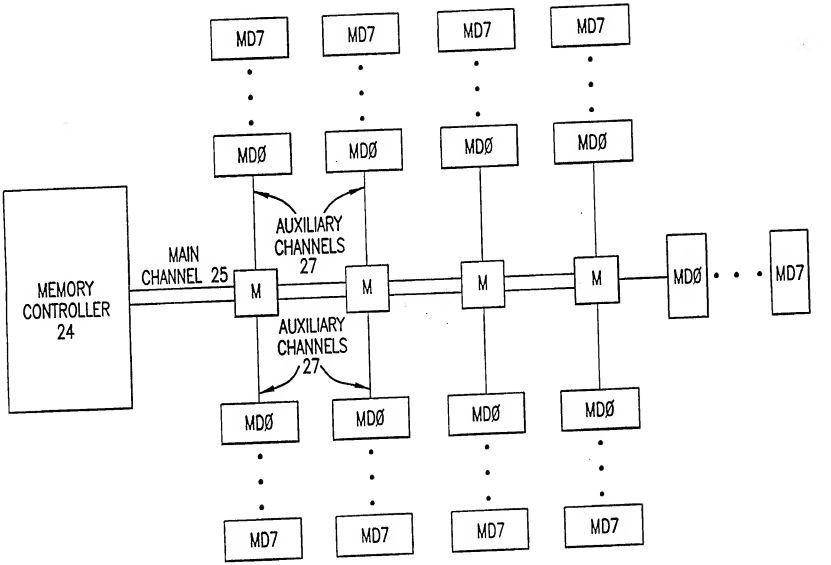

MD7
MD7
MD7
MD7
MDØ
MDØ
MDØ
MDØ
MEMORY CONTROLLER 24
MAIN CHANNEL 25
AUXILIARY CHANNELS 27
M
M
M
M
MDØ
MD7
AUXILIARY CHANNELS 27
MDØ
MDØ
MDØ
MDØ
MD7
MD7
MD7
MD7

FIG. 6

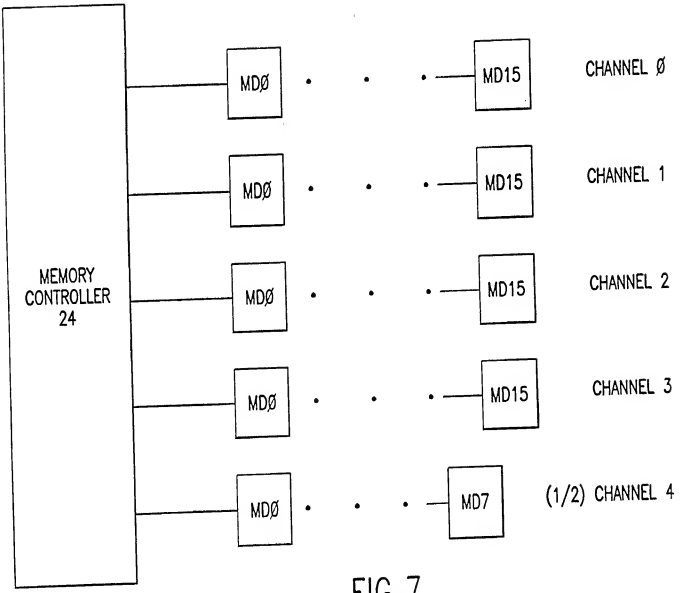

MEMORY CONTROLLER 24
MDØ
MD15
CHANNEL Ø
MDØ
MD15
CHANNEL 1
MDØ
MD15
CHANNEL 2
MDØ
MD15
CHANNEL 3
MDØ
MD7
(1/2) CHANNEL 4

FIG. 7

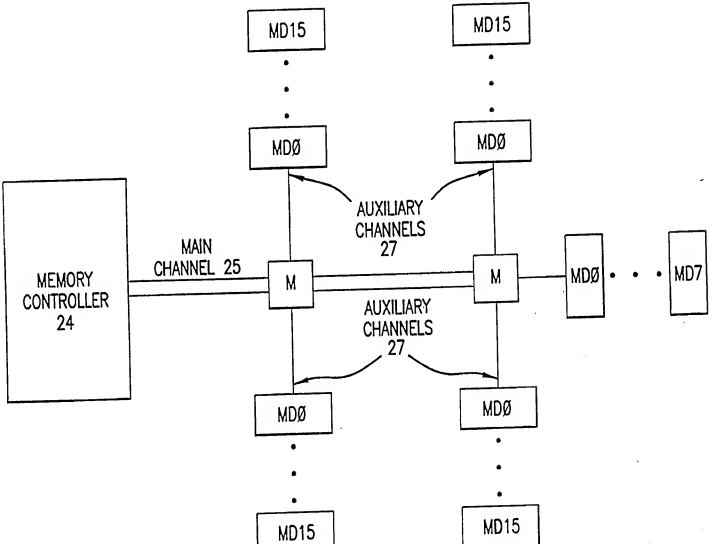

MD15
MD15
MDØ
MDØ
AUXILIARY
CHANNELS
27
MEMORY
CONTROLLER
24
MAIN
CHANNEL 25
M
M
MDØ
MD7
AUXILIARY
CHANNELS
27
MDØ
MDØ
MD15
MD15

FIG. 8

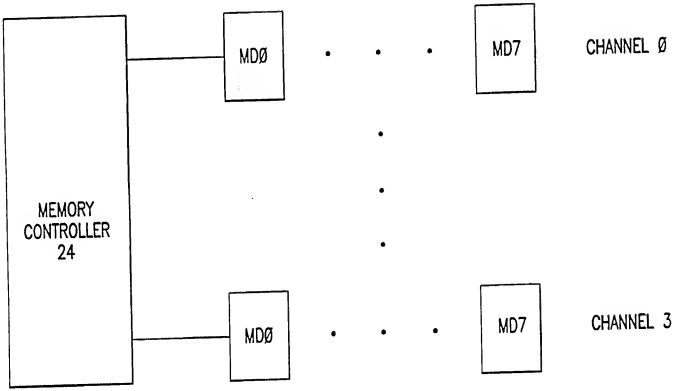


FIG. 9

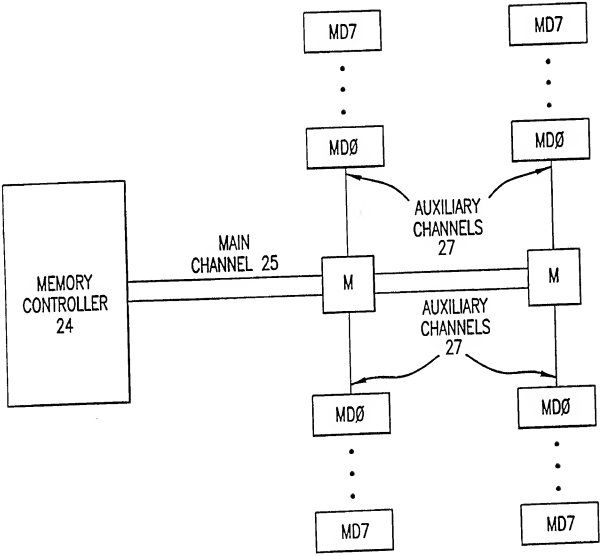

MD7
MD7
MDØ
MDØ
AUXILIARY
CHANNELS
27
MAIN
CHANNEL 25
MEMORY
CONTROLLER
24
M
M
AUXILIARY
CHANNELS
27
MDØ
MDØ
MD7
MD7

FIG. 10

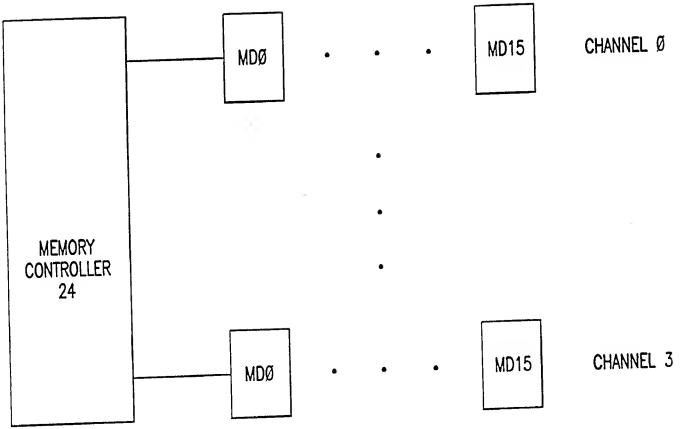


FIG. 11

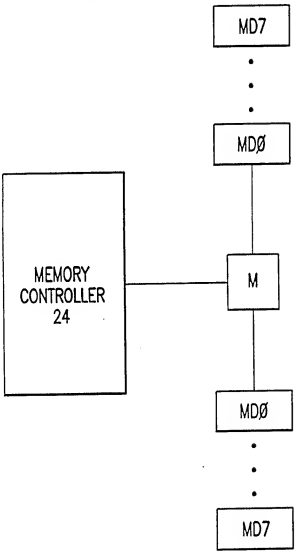


FIG. 12

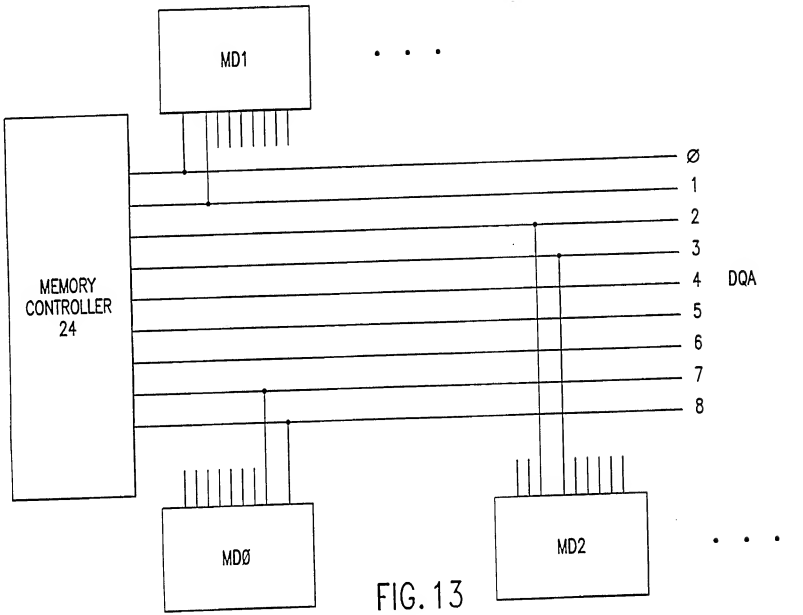
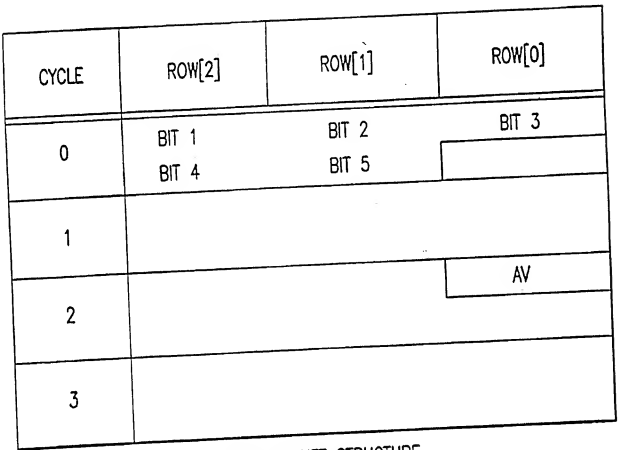
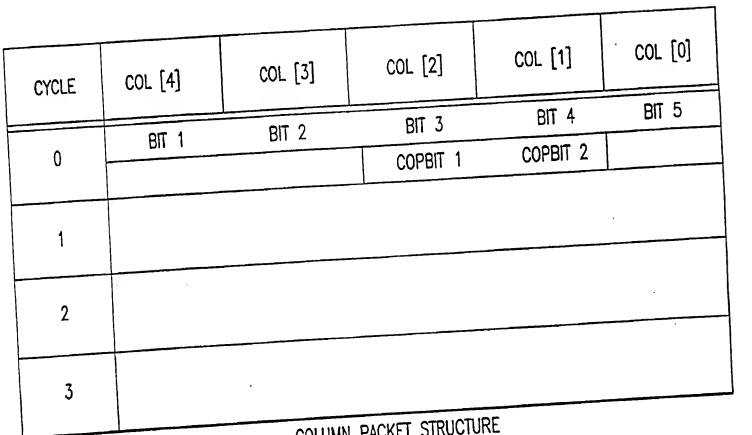


FIG. 13



ROW PACKET STRUCTURE

FIG. 14A



COLUMN PACKET STRUCTURE

FIG. 14B

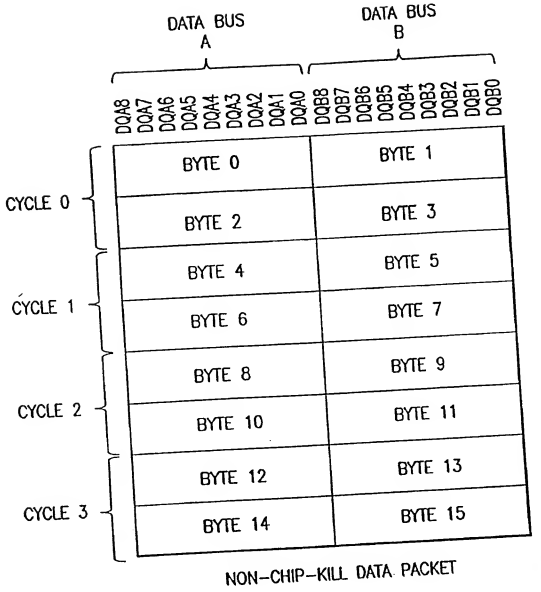

DATA BUS A
DATA BUS B
DQA8 DQA7 DQA6 DQA5 DQA4 DQA3 DQA2 DQA1 DQA0
DQB8 DQB7 DQB6 DQB5 DQB4 DQB3 DQB2 DQB1 DQB0
CYCLE 0
CYCLE 1
CYCLE 2
CYCLE 3
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
BYTE 8
BYTE 9
BYTE 10
BYTE 11
BYTE 12
BYTE 13
BYTE 14
BYTE 15
NON-CHIP-KILL DATA PACKET

FIG. 15

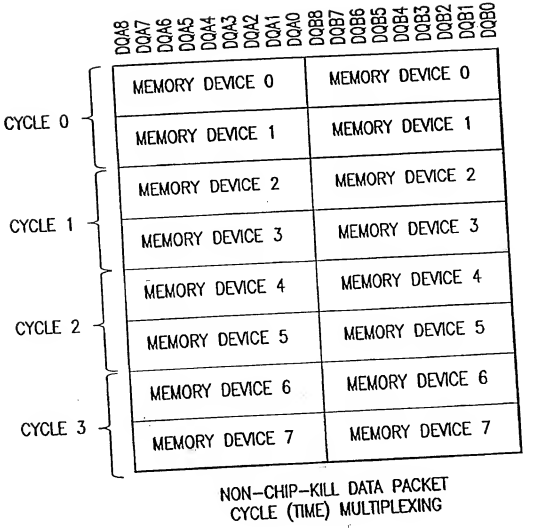

DQA8
DQA7
DQA6
DQA5
DQA4
DQA3
DQA2
DQA1
DQA0
DQB8
DQB7
DQB6
DQB5
DQB4
DQB3
DQB2
DQB1
DQB0
CYCLE 0
CYCLE 1
CYCLE 2
CYCLE 3
MEMORY DEVICE 0
MEMORY DEVICE 0
MEMORY DEVICE 1
MEMORY DEVICE 1
MEMORY DEVICE 2
MEMORY DEVICE 2
MEMORY DEVICE 3
MEMORY DEVICE 3
MEMORY DEVICE 4
MEMORY DEVICE 4
MEMORY DEVICE 5
MEMORY DEVICE 5
MEMORY DEVICE 6
MEMORY DEVICE 6
MEMORY DEVICE 7
MEMORY DEVICE 7
NON-CHIP-KILL DATA PACKET
CYCLE (TIME) MULTIPLEXING

FIG. 16